IR-2300 (2-3077)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF APPEAL AND INTERFERENCES

In re Patent Application of

Richard Bullock et al.

Serial No.: 09/773,872

Filed: February 2, 2001

Date: July 29, 2004

Group Art Unit: 2812

Examiner: Richard A. Booth

For: METHOD OF FABRICATING A GATE DIELECTRIC LAYER FOR A THIN FILM TRANSISTOR

Mail Stop Appeal - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF UNDER 37 CFR §1.192

Sir:

This Appeal stems from the Examiner's final rejection dated October 29, 2003, in connection with the above-identified application. The Notice of Appeal was filed in the United States Patent and Trademark Office on April 29, 2004.

Status of Claims

Claims 1-19 are rejected and pending on appeal herein.

Real Party in Interest

The real party in interest is the assignee, International Rectifier Corporation.

Related Appeals and Interferences

The applicant, the assignee and the undersigned attorneys are not aware of any related appeals or interferences.

Status of Amendments

All amendments have been entered, the last amendment being a response entered subsequent to final rejection, dated January 29, 2004.

Summary of the Invention

The present invention is directed to the method of fabricating a gate dielectric layer for a thin film transistor. Thin film transistors (TFTs), as suggested by their name, are thin semiconductor devices typically used in liquid crystal display (LCD) panels to switch photo transmitters to provide an image on a display screen. TFTs typically have a gate terminal for receiving a signal to switch the TFT on or off. The gate itself is composed of semiconductor material that causes an underlying active polysilicon layer to change state to permit or prevent conduction. The gate semiconductor material is separated from the underlying active polysilicon layer by a gate dielectric layer that provides certain insulating qualities. For example, the gate dielectric layer contributes to increasing a breakdown voltage and reducing leakage current to make the TFT more effective and efficient.

The active polysilicon region of a TFT is comparatively rough with respect to single crystalline silicon and has a bumpy or uneven surface due to the contour of numerous small silicon grains making up the polysilicon region. Accordingly, when a gate dielectric layer is formed over the uneven polysilicon surface the performance of the TFT can be inconsistent. The gate dielectric layer is typically formed of an oxide, such as silicon dioxide, and should provide a good barrier between the gate and the underlying active polysilicon layer to provide good insulative qualities. However, due to the uneven polysilicon layer, the capability of the gate dielectric layer to provide proper performance is compromised because the layer is necessarily

thinner in some areas and thicker in others due to the unevenness of the underlying polysilicon layer. Where the gate dielectric layer is thinner, the oxide is less capable of providing a high gate breakdown voltage and a low gate leakage current. This problem is much less prevalent in semiconductor devices where a single crystalline silicon underlies a dielectric layer, because single crystal silicon is orders of magnitude smoother than the rougher polysilicon layer.

To solve the problem of inadequate parametric performance occurring through low gate breakdown voltage and high gate leakage current in TFT devices where the gate dielectric layer overlying the polysilicon layer is inconsistent in its thickness, the present invention provides a technique for forming the gate dielectric layer to improve parametric performance. In one embodiment a composite dielectric layer is formed that meets the device specifications desired through a novel process provided to one or more of a plurality of dielectric layers. In another embodiment, the present invention provides a single dielectric layer that is formed according to the novel process.

In the first embodiment, a thin dielectric layer using silicon dioxide as a dielectric is deposited over the rough polysilicon surface to obtain a surface that is more consistent and smoother than the underlying rough polysilicon surface. The gate dielectric layer is thermally grown over the rough polysilicon layer. The growth of the first dielectric layer is then followed by an anneal procedure that improves the parametric performance of the TFT device because the anneal tends to produce smaller polysilicon grains and a more consistent dielectric layer. The first dielectric layer is then overlaid by a second dielectric layer that is also thermally grown and is designed to provide the parametric performance to meet the specifications of the intended device. The thermal growth of the second dielectric layer is followed by another anneal cycle, which tends to decrease the porosity of the second dielectric layer and thereby improve the parametric performance of the overall device. A gate semiconductor material is then deposited over the composite gate dielectric layer, patterned and finished according to conventional techniques to produce a complete TFT device.

According to the second embodiment of the present invention, a thick gate dielectric layer is deposited over the rough polysilicon layer and is thermally grown to a desired thickness. After thermal growth of the gate dielectric layer, an anneal procedure is performed, which again tends

to reduce the size of the polysilicon grains to improve parametric performance while decreasing the porosity of the gate dielectric layer. After deposition of the gate semiconductor material, patterning and finishing, a complete TFT device is produced.

In the first embodiment, the TFT device produced exhibits greatly improved parametric performance over TFT devices with a single gate dielectric layer thermally deposited on an underlying active layer without an anneal step. In the second embodiment, improved parametric performance is achieved with fewer steps than in the first embodiment over TFT devices with a single thermally grown dielectric layer deposited over an active layer without an anneal step.

Issues on Appeal

(1) Whether claims 16-19 are rendered obvious under 35 U.S.C. §103(a) over the combination of Miyasaka (U.S. Patent No. 6,124,154) in view of Kuo et al. (U.S. Patent No. 5,981,347).

(2) Whether claims 1-19 are rendered obvious under 35 U.S.C. §103(a) over Huang et al. (U.S. Patent No. 6,037,199) in view of Doklan et al. (U.S. Patent No. 4,851,370) or Kuo et al.

Grouping of Claims

Claims 1-15 stand or fall together as Group 1 with respect to Issue 2.

Claims 16-19 stand or fall together as Group 2 with respect to Issue 2.

Argument

Briefly stated, it is applicant's position that none of the cited prior art references used to reject claims 1-19 on appeal in Groups 1 and 2, teach or suggest the deposition of a dielectric layer over a rough polysilicon layer that is formed on an insulating substrate, followed by an anneal step, where the thickness of the dielectric layer is in the range of from about 500 to about 700Å. In each of the cited prior art references, a dielectric layer is formed either over a single

crystalline silicon layer that is orders of magnitude smoother than the rough polysilicon layer used to form the TFT device according to the present invention, or the reference is silent as to an anneal step or the thickness of the dielectric layer. In addition, the present invention recited in claims 1-19 calls for specific step sequences and parameters that are not taught or suggested in the cited prior art references.

Issue 1

The Examiner states in the rejection of claims 16-19 under 35 U.S.C. §103(a) that Miyasaka shows an insulating substrate, an active semiconductor layer on the insulating substrate, a gate dielectric layer on the active semiconductor layer and performing an anneal procedure to densify the gate dielectric layer. The Examiner further states that Miyasaka lacks anticipation of specific processing conditions with respect to the polysilicon layer and the thermal oxidation and densification processes, as well as the performance of a first anneal procedure subsequent to growing a first dielectric layer. In this respect, the Examiner appears to be referring to the parameters stated in claims 16-19 for which the disclosure by Miyasaka is silent. For example, claim 16 recites a gate dielectric layer with a thickness of from about 500 to 700 Å, and performing a first anneal procedure after the formation of a polysilicon layer and an overlaid gate dielectric layer. Indeed, Miyasaka appears to be silent with regard to the parameters for forming a gate dielectric layer, including the thickness, deposition temperatures and annealing temperatures. Miyasaka is also silent with respect to the thickness of the semiconductor layer deposited on the insulating substrate, which is provided in the present application in claim 17.

The Examiner therefore seeks to supply the missing elements that are not anticipated by Miyasaka from the disclosure by Kuo et al., in an obvious combination.

The disclosure by Kuo et al., however, calls for the formation of a gate dielectric layer with a thickness of about 65 to about 75 Å on the active region of the semiconductor substrate. Claim 16 of the present invention recites a gate dielectric layer thickness of about 500 to about 700Å, approximately an order of magnitude larger than the gate dielectric layer called for in the disclosure by Kuo et al. Accordingly, the disclosures by Miyasaka and Kuo et al. fail to teach or

suggest the limitations recited in claims 16-19, either alone or in combination with each other, and therefore do not support a *prima facie* case of obviousness against those claims.

Applicants further submit that because the disclosure by Miyasaka is silent with respect to the parameters for the gate dielectric layer, there is no suggestion or motivation to combine the disclosure by Miyasaka with that of Kuo et al. because the gate dielectric layer is not identified as being important with respect to parameter characteristics in the formation of the gate dielectric layer. Indeed, the recitation and the disclosure by Kuo et al. of a gate dielectric layer of about 65 to about 75Å argues against the combination of Miyasaka and Kuo et al. to arrive at the invention recited in claims 16-19 because of the substantial difference between the gate dielectric dimensions taught by Kuo et al. and those recited in claims 16-19 of the present invention. Indeed, if one of ordinary skill in the art were to combine the teachings of Miyasaka and Kuo et al. with respect to the gate dielectric layer, at most the gate dielectric layer with a thickness of about 65 to about 75Å would result. There would still be no teaching with respect to the gate dielectric deposition temperature or the annealing procedure temperature, as recited in claims 18 and 19, respectively. Moreover, the disclosures by Miyasaka and Kuo et al fail to provide any dimensions for the thickness of the polysilicon layer upon which the gate dielectric is overlaid, which is an element specified in claim 17. Applicants therefore submit that the disclosures by Miyasaka and Kuo et al. fail to teach or suggest the number of elements recited in claims 16-19, and that there is no suggestion or motivation to combine those references to achieve the recited invention.

In addition, the Examiner states that Kuo et al. disclose performing a high temperature anneal after gate oxide formation to activate the source/drain regions, which the Examiner apparently considers to be the same as performing an anneal procedure to densify a silicon oxide gate dielectric layer, as recited in claims 16-19. However, applicant first notes that the disclosure by Kuo et al. is silent with respect to the state of the semiconductor substrate material, that is, whether it is single crystal silicon, polysilicon, or amorphous silicon, for example. Kuo et al. do state that a formation of the gate dielectric layer is performed through thermal oxidation at a temperature of from about 750 to about 850°C, which is clearly outside the range recited in claim 18, for example, of about 600 to 700°C. The disclosure by Kuo et al. calls for a thermal

annealing temperature of from about 900 to about 950°C to activate the source/drain regions, where the thermal annealing reacting chamber employs a nitrogen annealing gas ambient. The annealing ambient gas is notable for the lack of oxygen, which would cause the further formation of a silicon oxide layer if present, which Kuo et al. must avoid to be able to form the activated source/drain regions. However, claim 19 specifically calls for an ambient comprised of a mixture of oxygen in either nitrogen or argon. Again, Kuo et al. fail to teach a number of elements recited in the rejected claims, either alone or in combination with the disclosure by Miyasaka, and therefore lacks support for a *prima facie* case of obviousness against those claims.

Applicants further note that although Kuo et al. appear to disclose a high temperature anneal, the annealing process is solely for the purpose of activating the source/drain regions. That is, Kuo et al. do not recognize the advantages or results of performing a high temperature anneal on a thick gate oxide layer, among other reasons, for the simple fact that Kuo et al. fail to disclose a thick gate oxide. Instead, Kuo et al. appear to be focused solely on activating the source/drain regions rather than bringing about any change to the gate dielectric layer.

Accordingly, applicants respectfully submit that the Examiner has not established the requirements for a *prima facie* case of obviousness because the cited prior art references do not suggest or motivate the combination or modification of their disclosures, all of the claim limitations are not taught in the cited references, either alone or in combination, and the disclosures by Miyasaka and Kuo et al. actually teach away from the present invention recited in claims 16-19. Furthermore, applicants note that because the disclosure by Kuo et al. is directed to a MOSFET, while that of Miyasaka is directed to a TFT, it would not be obvious to one of ordinary skill in the art to combine these references. The MOSFET disclosed by Kuo et al. is in all likelihood provided with a substrate that is monocrystalline silicon to achieve the performance parameters expected of typical MOSFET devices. This position is supported by the fact that Kuo et al. provide for a gate dielectric layer that has a thickness of about 65 to about 75Å, typical for MOSFET devices but approximately an order of magnitude smaller than the thickness of the gate dielectric layer recited in claims 16-19 of the present invention. However, the Examiner states in the Office Action section entitled Response to Arguments that Kuo et al. and the present application employ MOS based semiconductor devices, with the only difference being that these

devices are formed on different substrates. This statement appears to rely on the reasoning that if any type of MOS semiconductor device is taught in a prior art reference, then it would be obvious for the applicants to try to produce a MOS based device like that recited in claims 16-19 of the present invention. This "obvious to try" standard for determining obviousness is inappropriate in the absence of some objective reason or motivation to combine the teachings of the reference to arrive at the present invention recited in claims 16-19. The appropriate standard for a determination of obviousness is to determine the scope and contents of the prior art and the differences between the prior art and the claims at issue and to determine the level of ordinary skill in the relevant art. Applicants respectfully submit that the Examiner in this instance has applied an incorrect standard of obviousness in arriving at the conclusion of rejecting claims 16-19 as evidenced by the comments in the Office Action.

Applicants also note that the Yamazaki reference (U.S. Patent No. 6,306,213) is not used to reject claims 16-19, although it is cited for the proposition that a thick gate dielectric layer is known in the art. Because the Yamazaki reference is not used to reject claims 16-19, however, it should not be considered as supporting a *prima facie* case of obviousness against claims 16-19.

The Examiner states that official notice is taken that the parameters recited in claims 16-19 are typical well known processing conditions suitable for forming dielectric layers and performing oxide densification. Applicants have previously challenged the Examiner on this conclusion to provide evidence in support of the conclusion of obviousness, as is required. MPEP §2142 ("With regard to rejections under 35 U.S.C. §103, the Examiner must provide evidence which as a whole shows that the legal determination sought to be proved (i.e., the reference teachings establish a *prima facie* case of obviousness) is more probable than not.") In the present case, the Examiner has failed to supply evidence in the rejection of claims 16-19 in support of a legal determination of obviousness with respect to the parameter ranges recited in claims 16-19. Although applicants requested evidence in support of the Examiner's official notice that the recited parameters are typical well known processing conditions, none has been forthcoming. Although the Examiner cites Yamazaki in support of the official notice taken of the parameter ranges recited in claims 16-19, and although the Examiner states that in view of the disclosure by Yamazaki it would have been obvious to one of ordinary skill in the art that a

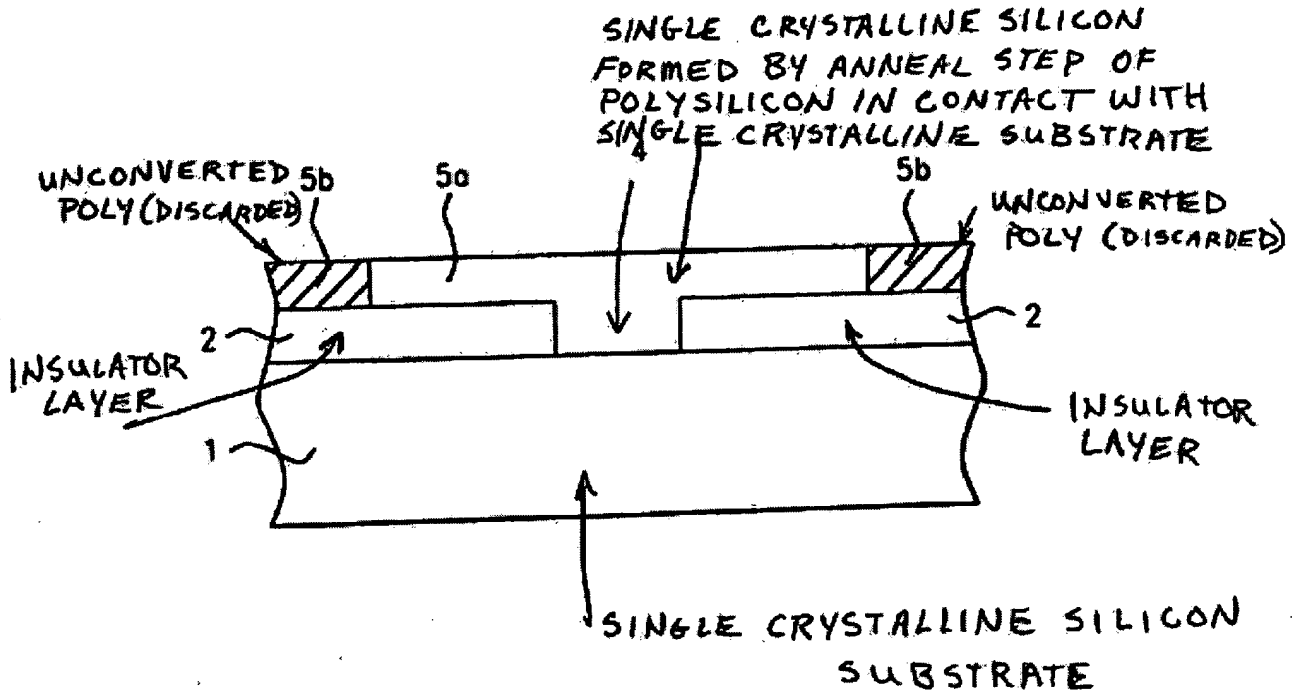
prima facie case of obviousness exists with respect to forming a gate dielectric with a thickness ranging from 550-850Å, the Yamazaki reference is not used to reject claims 16-19 and should therefore not be considered to anticipate or make obvious the invention recited in claims 16-19.

Accordingly, in view of the above discussion, applicants respectfully submit that claims 16-19 are allowable over the cited prior art references, either alone or in combination with each other, or knowledge generally available to one of ordinary skill in the art. Applicants therefore respectfully request that the rejection of claims 16-19 under 35 U.S.C. §103(a) be reversed.

Issue 2

The Examiner states in the Office Action that claims 1-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Huang et al. in view of Doklan et al. or Kuo et al. In particular, the Examiner cites the disclosure by Huang et al. as providing a number of elements recited in claims 1-19. For example, the Examiner states that Huang et al. show an insulating substrate designated with reference numeral 1. A review of the disclosure by Huang et al. indicates a substrate designated with reference numeral 1 is a "P type, semiconductor substrate 1, comprised of single crystalline silicon, with a <100> crystallographic orientation," which is clearly not an insulating substrate as is recited in claims 1-19.

The Examiner also states that Huang et al. disclose an active semiconductor layer of polysilicon with a thickness of 300-1000Å. While the disclosure by Huang et al. does indeed appear to call for a layer of polysilicon initially deposited over an insulator layer designated with reference numeral 2, the subsequent steps performed by Huang et al. converts the polysilicon layer to a single crystalline layer designated with reference numeral 5a as a result of an anneal step of the polysilicon where the polysilicon in contact with single crystalline substrate 1 acts as a seed. An annotated figure of the structure disclosed by Huang et al. is provided below.



The Examiner also states that a gate dielectric layer is formed on the polysilicon layer, designated with reference numeral 9. However, Figures 6 and 7 of the disclosure by Huang et al. clearly show a gate dielectric layer with a thickness of between about 30 to 100Å overlies a single crystalline layer designated with reference numeral 5c.

Accordingly, the disclosure by Huang et al. lacks a number of elements that are recited in claims 1-19, including the provision of an insulating substrate, a rough polysilicon layer on the insulating substrate and a first gate dielectric layer thermally grown on the polysilicon layer. The Office Action also states that Huang et al. lacks anticipation for forming a composite gate dielectric layer comprising a first thermally grown oxide layer followed by an annealing process and a second thermally deposited oxide layer using TEOS as a source followed by a subsequent anneal. The Examiner states that the above deficiencies with respect to the disclosure by Huang

et al. are overcome with respect to the recitation of the invention found in claims 1-19 by Doklan et al. or Kuo et al. In particular, the Examiner states that Doklan et al. teach a first thermally grown oxide layer over a polysilicon substrate followed by the deposition of an oxide layer using TEOS, with anneal processes conducted after the formation of each oxide layer.

Claims 1-6 of the present invention recite:

> thermally growing a first gate dielectric layer, in a furnace, on said polysilicon layer;
>
> subsequent to growing said first gate dielectric layer, performing a first anneal procedure to change said polysilicon layer.

Nowhere in the disclosure by Doklan et al. is there a teaching or suggestion to modify a polysilicon layer through an anneal procedure conducted after the thermal growth of a first gate dielectric layer in a furnace. Claims 1-6 also recite that the composite gate dielectric layer formed from the first and second gate dielectric layers has a thickness of from about 550 to 850Å, while Doklan et al. appears to teach a composite oxide layer of at most 100Å. As discussed above, none of these elements are taught or suggested in the disclosure by Huang et al. Accordingly, claims 1-6 include a number of recitations that are not found in the disclosures by Huang et al. or Doklan et al., either alone or in combination. Because these cited prior art references do not teach each and every element recited in claims 1-6, a *prima facie* case of obviousness may not be established.

Claims 7-15 of the present invention recite:

> thermally growing a first silicon oxide layer, in a furnace on said polysilicon layer;
>
> subsequent to growing said first silicon oxide layer, performing a first anneal procedure in situ in said furnace, to improve TFT parametric performance.

As discussed above, claims 7-15 recite a number of elements not found in the disclosure by Huang et al., and the above cited elements are not disclosed by Doklan et al. That is, Doklan et al. fail to teach or suggest a growth of a silicon oxide layer over a polysilicon layer and the performance of a first anneal procedure in situ in the furnace in which the first silicon oxide layer was formed. Moreover, claims 7-15 recite that the composite gate dielectric layer formed from the first and second silicon oxide layers has a thickness of from about 550 to 850Å. As noted above, Doklan et al. appear to teach a composite dielectric layer with a thickness of at most 100Å.

Accordingly, the disclosures by Huang et al. and Doklan et al. fail to teach a number of claim limitations recited in claims 7-15, either alone or in combination, and therefore do not support a *prima facie* case of obviousness with respect to those claims.

Claims 16-19 recite the steps of:

> providing an insulating substrate;
>
> forming a rough polysilicon layer on said insulating substrate;
>
> thermally depositing a silicon oxide gate dielectric layer on said polysilicon layer, using tetraethylorthosilicate as a source to a thickness of from about 500 to 700Å.

As discussed above, the disclosures by Huang et al. and Doklan et al. fail to teach a number of elements recited in claims 16-19, including the provision of an insulating substrate, the formation of a rough polysilicon layer on the insulating substrate and the deposition of a silicon oxide gate dielectric layer on a polysilicon layer where the thickness of the gate dielectric layer is about 500 to 700Å. Accordingly, the disclosures by Huang et al. and Doklan et al. do not teach all of the claim limitations recited in claims 16-19, either alone or in combination, and therefore do not support a *prima facie* case of obviousness with respect to those claims.

Turning to the rejection of claims 1-19 under 35 U.S.C. §103(a) over the disclosures by Huang et al. in view of Kuo et al., applicants note that claims 1-15 recite the formation of a composite gate dielectric layer, which is completely absent from the disclosures by Huang et al.

and Kuo et al. With respect to claims 16-19, applicants note that the disclosures by Huang et al. and Kuo et al. fail to disclose or suggest an insulating substrate over which is formed a polysilicon layer that is then overlaid by a gate dielectric layer with a thickness of about 500 to 700Å. As noted previously, Huang et al. appear to teach a gate dielectric layer overlaying a single crystalline silicon layer and the thickness of the gate dielectric layer is approximately 30 to 100Å. Similarly, the disclosure by Kuo et al. calls for a gate dielectric layer having a thickness of about 65 to about 75Å, which like the disclosure by Kuo et al., is an order of magnitude smaller than the gate dielectric layer called for in claims 16-19. The disclosure by Kuo et al. also appears to lack any teaching or suggestion for the deposition of a gate dielectric layer over a polysilicon layer, but rather appears to utilize single crystalline silicon to form the disclosed MOSFET device. Accordingly, the disclosures by Huang et al. and Kuo et al. fail to teach or suggest the number of elements recited in claims 16-19 of the present invention, and therefore do not support a *prima facie* case of obviousness.

The Examiner also states that Kuo et al. discloses performing a high temperature anneal after a gate oxide formation to activate a source/drain region and takes the view that such an anneal would inherently include the oxide layer provided over the silicon substrate in the MOSFET disclosed by Kuo et al. As noted above, applicants submit that such a conclusion does not rely a proper application of the standard for obviousness under 35 U.S.C. §103. The disclosure by Kuo et al. fails to identify a range or results expected by annealing a gate dielectric layer. Kuo et al. also fail to teach a gate dielectric layer that has a thickness of from about 500 to 700Å, as is recited in claims 16-19 of the present invention, as well as failing to recite an insulating substrate overlaid by a rough polysilicon layer, which is overlaid by the gate dielectric layer. Indeed, for these reasons the disclosure by Kuo et al. appears to teach away from the invention recited in claims 16-19 for at least the reason that the thickness of the gate dielectric is an order of magnitude larger in the claims of the present invention than the gate dielectric layer described by Kuo et al. One of ordinary skill in the art would not be taught to arrive at a gate dielectric layer with a thickness of about 500 to 700Å overlaying a rough polysilicon layer overlaying an insulating substrate based on the disclosures by Huang et al. and Kuo et al., either alone or in combination. Accordingly, applicants respectfully submit that a *prima facie* case of

obviousness has not been established with respect to claims 16-19 over the disclosures by Huang et al. and Kuo et al. either alone or in combination.

With respect to the rejection of claims 1-19 under 35 U.S.C. §103(a) over the disclosures by Huang et al. in view of Doklan et al. or Kuo et al., applicants respectfully submit that there is no motivation, suggestion or teaching to combine the references to arrive at the present invention recited in claims 1-19. As noted above, Huang et al. fail to teach a number of elements recited in claims 1-19, including an insulating substrate, a layer of polysilicon over an insulating substrate and a gate dielectric layer over a polysilicon layer. The disclosure by Doklan et al. appears to teach a composite dielectric layer for the reduction of defects in the structure, where the composite dielectric is no more than approximately 100Å thick. The disclosure by Huang et al. discloses no difficulty or issue with gate dielectric voltage breakdown or leakage current and therefore lacks any suggestion or motivation to modify the gate dielectric layer to increase the complexity of formation, for example, as illustrated by the disclosure by Doklan et al. Doklan et al. also fail to teach or suggest a thickened composite dielectric layer so that one of ordinary skill would learn only a composite oxide layer, with a thickness that is within the range stated in the disclosure by Huang et al. of about 30 to 100Å. Indeed, the disclosure by Huang et al. is focused on a process for the formation of DRAM cells in SOI segments and does not teach, suggest or motivate one of ordinary skill in the art to modify a gate dielectric layer in accordance with the disclosure by Doklan et al.

There is also no teaching, suggestion or motivation to combine the references by Huang et al. and Kuo et al. with respect to the invention recited in claims 1-19. As stated above, the disclosures by Huang et al. and Kuo et al. lack a number of elements recited in claims 1-19, either alone or in combination. In addition, one of ordinary skill in the art seeking to construct a TFT device would not look to the disclosures by Huang et al. or Kuo et al., either alone or in combination, and would receive no motivation or suggestion to combine the references because of their lack of comparability. That is, in order to be motivated to combine the disclosures of Huang et al. and Kuo et al., one of ordinary skill in the art would have to seek to establish a hot carrier effect (HCE) resistant activated MOSFET in a DRAM cell constructed of SOI segments rather than a TFT device. There is no such suggestion or motivation in the disclosure by Huang

et al. to form a TFT device. Similarly, there is no suggestion or motivation in the disclosure by Kuo et al. to form DRAM cells in SOI segments, since the disclosure by Kuo et al. and the problem to be solved is directed to an issue related to power MOSFETs that control a significant amount of current or voltage. The detrimental effects of HCE sought to be reduced in the disclosure by Kuo et al. are inapplicable to the device disclosed by Huang et al. Accordingly, there is no teaching, suggestion or motivation to combine the references by Huang et al. and Kuo et al. to support a *prima facie* case of obviousness.

For all of the above reasons, applicants respectfully submit that the cited prior art references fail to teach or suggest a number of elements recited in claims 1-19, either alone or in combination, and therefore fail to establish a *prima facie* case of obviousness. In addition, applicants respectfully submit that there is no teaching, suggestion or motivation to combine the references cited in an effort to produce the invention recited in claims 1-19. For all the above reasons, applicants respectfully submit that the rejection of claims 1-19 under 35 U.S.C. §103(a) of the disclosures by Huang et al. and Doklan et al. or Kuo et al. be reversed.

Applicants note that claims 1-6 and 7-15 recite a first method for forming a composite gate dielectric layer and a thin film transistor, respectively, and should be considered to stand or fall together. The novel composite gate dielectric layer recited in claims 1-6 is also incorporated into claims 7-15, with the additional recitations in claims 7-15 describing the complete formation of a TFT. Accordingly, if claim 1 is selected from Group 1 as represented of the group, claims 1-15 understandably stand or fall together.

Claims 16-19, unlike claims 1-15, recite a simplified technique for forming a gate dielectric layer that should be separately patentable. For example, claims 16-19 call for a single anneal step to densify the gate dielectric layer, which is significantly less complicated than the composite gate dielectric layer construction recited in claims 1-15. For these reasons, claims 1-15 in Group 1 and claims 16-19 in Group 2 should not be considered to stand or fall together, but rather should be examined separately on their own merits.

Conclusion

In view of the foregoing, it is respectfully submitted that claims 1-19 are clearly patentable over the cited references. Applicants therefore respectfully request that the Examiner's rejection of claims 1-19 be reversed and that the application be passed to issue.

Our Check No. 17636 which includes the amount $330.00 to cover the filing of the appeal brief is attached hereto. This brief is being submitted in triplicate in accordance with 37 CFR 1.192 and applicants reserves the right to request an oral hearing upon receipt of the Examiner's Answer.

If this communication is being filed after a shortened statutory time period has elapsed and no separate petition is enclosed, the Commissioner of Patents and Trademarks is petitioned under 37 CFR §1.36(a) to extend the time for filing the required paper by the number of months which will avoid abandonment under 37 CFR §1.135. The fee under 37 CFR 1.17 should be charge to our Deposit Account No. 15-0700.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Appeal - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 29, 2004:

Brendan J. Kennedy
Name of applicant, assignee or Registered Representative

Brendan J. Kennedy
Signature

July 29, 2004
Date of Signature

Respectfully submitted,

Brendan J. Kennedy
Registration No.: 41,890
OSTROLENK, FABER, GERB & SOFFEN, LLP
1180 Avenue of the Americas
New York, New York 10036-8403
Telephone: (212) 382-0700

BJK:gl

CLAIMS ON APPEAL

1. A method of forming a composite gate dielectric layer for a thin film transistor (TFT), device, comprising the steps of:

providing an insulating substrate;

providing a rough polysilicon layer on said insulating substrate;

thermally growing a first gate dielectric layer, in a furnace, on said polysilicon layer;

subsequent to growing said first gate dielectric layer, performing a first anneal procedure to change said polysilicon layer;

thermally depositing a second gate dielectric layer on said first gate dielectric layer; and

performing a second anneal procedure to create a densified second gate dielectric layer, resulting in said composite gate dielectric layer comprised of said densified second gate dielectric on said first gate dielectric layer, said composite gate dielectric layer having a thickness of from about 550 to 850 Angstroms.

2. The method of claim 1, wherein said polysilicon layer is obtained via low pressure chemical vapor deposition (LPCVD) procedures to a thickness of from about 500 to 1000 Angstroms.

3. The method of claim 1, wherein said first gate dielectric layer is a silicon oxide layer, at a thickness between about 50 to 150 Angstroms, obtained via thermal oxidation procedures, performed in an ambient comprised of a mixture of oxygen in either argon or nitrogen, at a temperature between about 800 to 1100°C, and performed for a time between about 15 to 30 min.

4. The method of claim 1, wherein said first anneal procedure, used to change said polysilicon layer, is performed at a temperature between about 900 to 1200°C, in a nitrogen or argon ambient, for a time between about 3 to 5 hrs.

5. The method of claim 1, wherein said second gate dielectric layer is a thermally deposited silicon oxide layer, obtained at a thickness between about 500 to 700 Angstroms, deposited at a temperature between about 600 to 700°C, using tetraethylorthosilicate as a source.

6. The method of claim 1, wherein said second anneal procedure, used to create said densified second gate dielectric layer, is performed at a temperature between about 900 to 1000°C, in an ambient comprised of a mixture of oxygen in either nitrogen or argon.

7. A method forming a thin film transistor, featuring a composite gate dielectric layer, on an insulating substrate, comprising the steps of:

providing said insulating substrate;

forming a first rough polysilicon layer on said insulating substrate;

thermally growing a first silicon oxide layer, in a furnace, on said polysilicon layer;

subsequent to growing said first silicon oxide layer, performing a first anneal procedure, in situ in said furnace, to improve TFT parametric performance;

thermally depositing a second silicon oxide gate dielectric layer, on underlying, said first silicon oxide dielectric layer, via thermal decomposition of tetraethylorthosilicate (TEOS),

performing a second anneal procedure to densify said second silicon oxide gate dielectric layer, resulting in said composite gate dielectric layer, comprised of densified, said second silicon oxide gate dielectric layer on said first silicon oxide gate insulator layer, said composite gate dielectric layer having a thickness of from about 550 to 850 Angstroms;

depositing a second polysilicon layer;

patterning of said second polysilicon layer, and of said composite gate dielectric layer to create a polysilicon gate structure on said composite gate dielectric layer; and

forming a source/drain region in a portion of said first polysilicon layer, not covered by said polysilicon gate structure.

8. The method of claim 7, wherein said first polysilicon layer is obtained via low pressure chemical vapor deposition (LPCVD) procedures, to a thickness between about 500 to 1500 Angstroms.

9. The method of claim 7, wherein said first silicon oxide gate dielectric layer is thermally grown to a thickness between about 50 to 150 Angstroms, via thermal oxidation procedures performed

in an ambient comprised of a mixture of oxygen in either argon or nitrogen, at a temperature between about 800 to 1100°C, and for a time between about 15 to 30 min.

10. The method of claim 7, wherein said anneal procedure, used to improve TFT parametric performance, is performed at a temperature between about 900 to 1200°C, in a nitrogen or argon ambient, for a time between about 3 to 5 hrs.

11. The method of claim 7, wherein said second silicon oxide gate dielectric layer is a thermally deposited silicon oxide layer, obtained at a thickness between about 500 to 700 Angstroms, deposited at a temperature between about 600 to 700°C, using tetraethylorthosilicate as a source.

12. The method of claim 7, wherein said second anneal procedure, used to densify said second silicon oxide gate dielectric layer, is performed at a temperature between about 900 to 1000°C, in an ambient comprised of a mixture of oxygen, in either nitrogen or argon.

13. The method of claim 7, wherein said second polysilicon layer is obtained via low pressure chemical vapor deposition (LPCVD), procedures, at a thickness between about 3000 to 5000 Angstroms, and either doped in situ, during deposition, via the addition of arsine, or phosphine, to a silane ambient, or doped using PH_3 or $POCl_3$ source in a diffusion tube, or deposited intrinsically then doped via implantation of arsenic or phosphorous ions.

14. The method of claim 7, wherein said polysilicon gate structure, on said composite gate dielectric layer, is formed via a reactive ion etching procedure, using Cl_2 or SF_6 as an etchant for said second polysilicon layer, while using CF_4 or CHF_3 as an etchant for said composite gate dielectric layer.

15. The method of claim 7, wherein said source/drain region is formed via implantation of arsenic or phosphorous ions, at an energy between about 50 to 100 KeV, at a dose between about 1E15 to 1E16 atoms/cm^2.

16. A method of forming a thermally deposited, gate dielectric layer, for a thin film transistor device, comprising the steps of:

providing an insulating substrate;

forming a rough polysilicon layer on said insulating substrate;

thermally depositing a silicon oxide gate dielectric layer on said polysilicon layer, using tetraethylorthosilicate as a source to a thickness of from about 500 to 700 Angstroms; and

performing an anneal procedure to densify said silicon oxide gate dielectric layer.

17. The method of claim 16, wherein said polysilicon layer is obtained via low pressure chemical vapor deposition (LPCVD) procedures to a thickness of from about 500 to 1500 Angstroms.

18. The method of claim 16, wherein said silicon oxide gate dielectric layer is deposited at a temperature between about 600 to 700°C.

19. The method of claim 16, wherein said anneal procedure, used to densify said silicon oxide gate dielectric layer, is performed at a temperature between about 900 to 1000°C, in an ambient comprised of a mixture of oxygen in either nitrogen or argon.